University of Bahrain
College of Information Technology
Department of Computer Engineering

ITCE 202: Digital Logic
Test 1

Time: 1:00 hour

Date: November 2nd, 2004

Question	Marks	Score
1	24	
2	18	
3	18	
4	20	
5	20	
Total	100	

ID. No.	Name:	Sec.:

Show all your work.

Q1 (24 points)

(4 points) (a) Convert $(326.5)_8$ to Hexadecimal

(4 points) (b) The following number 1 1 1 0 0 0 0 1 1 0 0 1 0 1 1 1 represents decimal digits in 4-3-2-1 weighted code. Find its equivalent in BCD weighted code.

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(8 Points) (c) Divide in binary 1 1 1 0 1 00 by 1 0 1 0 and approximate the result up to two fraction bits.

(8 Points) (d) Perform the binary addition of the two decimal numbers (+39) and (-28), assume that the numbers are represented in 2's complement form.

Q2- (18 points)

(10 Points) (a) Simplify the following function to a minimum Sum of product form

$$Z = A\,\overline{B}\,C + F + (A\,\overline{B}\,D + C\,\overline{D})(\overline{C}\,E + \overline{F} + A\,\overline{B}\,D)$$

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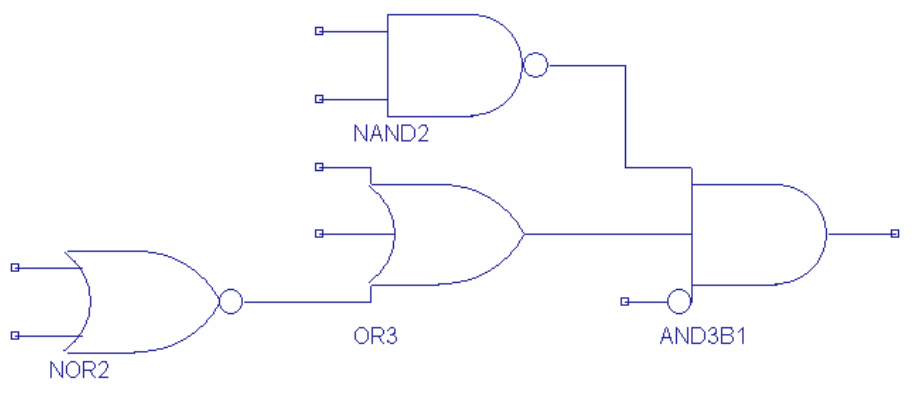
(8 Points) (b) Given that: $Z = \overline{EG}\,(A \oplus B + \overline{CE})(\overline{A} + BG)$

Use De'Morgan's Theorem to find $\overline{Z}$. Express your answer in a sum of product form (Do not simplify).

Q3 (18 points)

For the circuit shown in figure 1, find:



(10 Points) (a) Z in a standard Sum of product (minterm form)

(8 Points) (b) $\overline{Z}$ in a standard product of sums (algabric form).

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Q4 (20 points)

Realised the function Z given by the following equation using the minimum number of 2-inputs NAND gates only.

$$Z = \overline{A}\,B\,C\,\overline{D} + E\,\overline{F} + B\,\overline{D}\,\overline{G} + B\,\overline{D}\,\overline{E}$$

Q5- (20 points)

Given the Boolean function: $F = \overline{A}CD + AB\overline{CD} + ABC + ACD + \overline{A}B\overline{C}D$

Assuming that the inputs ABCD = 0000, ABCD = 1000, and ABCD = 1101 never occur, find a minimum NOR-NOR network implementation for F.

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Test II

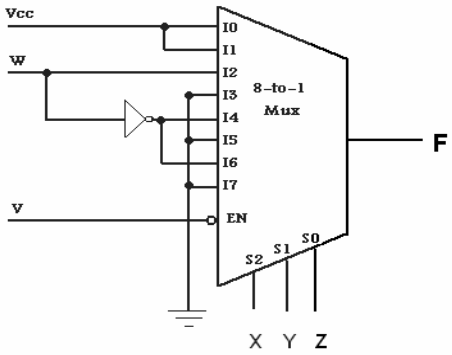
Time: 1:00 hour

Date: December 14, 2004

Question	Marks	Score
1	20	
2	20	
3	20	
4	20	
5	20	
Total	100	

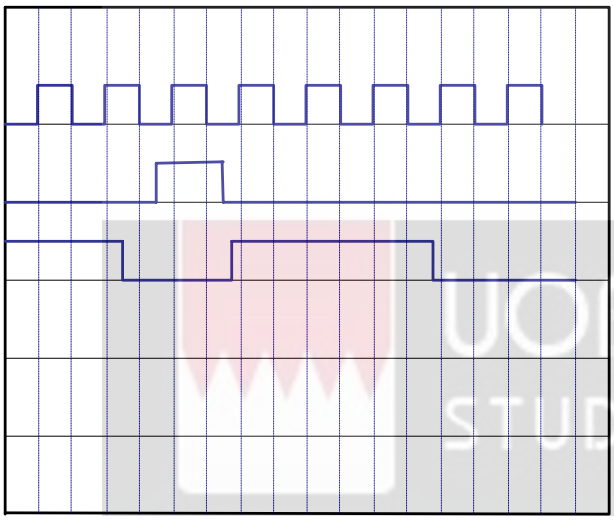
Q1 (20 points)
A combinational Logic Circuit accepts two 4-bit binary numbers $A = A_3\ A_2\ A_1\ A_0$, and $B = B_3\ B_2\ B_1\ B_0$ and generates a single output Z such that:
$Z = 1$ if $A + B + 7 \geq 12$ else $Z = 0$
Use any necessary ICs and logic gates to implement the combinational circuit.

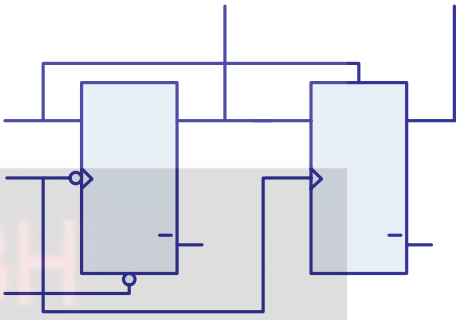
Q2(20 points)
Use 3-to-8 decoder(s) with enable to implement a code converter combinational circuit that takes as its inputs an Execss-3 code digit and outputs its equivalent BCD digit.



Q3 (20 points)
Express F in a S-O-P form (Do not simplify)

Q4(20 points)
Complete the following timing diagram for the circuit shown below.





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Q5(20 points)

A gated Latch has two inputs G, and L behaves as follows: If G = 0 the latch does not change its state. If G=1, the next state of the latch is equal to its input L

(a) Derive the characteristic equation of the G-L latch.

(b) Show how a J-K latch can be converted to a G-L latch.

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